

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having and composed of a plurality of unit data buses, ~~into which the data bus is divided and through each of which transfers data is transferred~~ concurrently;

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a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buses ~~bus in units of the unit data bus~~, and to use using said unit data bus ~~buses in unit data buses~~ requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said unit data bus ~~buses in unit data buses~~ for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses ~~bus in units of the unit data bus requested in unit data buses to said bus masters~~ in accordance with an said request signal, ~~availability of said data bus in units of the unit data bus~~, wherein

the request signal ~~and the grant signal has a data field comprising a plurality of bits,~~ each of said plurality of bits corresponding to a respective one of said unit data buses. ~~indicate identification or number of the unit data bus divided from the data bus.~~

Claim 2 (Currently Amended) The data transfer control circuit according to claim 1, wherein:

said bus controller sends gives the grant signal the use of said data bus to said bus masters ~~upon receipt based on of one of a request and a bus release requesting signal~~

requesting release of the use of said unit data buses. ~~bus in unit data buses inputted from said bus masters.~~

Claim 3 (Currently Amended) The data transfer control circuit according to claim 1, wherein:

 said bus controller includes a monitor circuit for monitoring ~~the availability of said data bus in~~ unit data buses.


Claim 4 (Currently Amended) The data transfer control circuit according to claim 3, wherein:

 said bus controller judges whether said ~~data bus is available in~~ unit data buses of said data bus are available based on a monitoring result by of said monitor circuit, and when said unit data bus is buses are available, said bus controller provides gives the grant signal of the use of said unit data buses ~~bus~~ to said bus master.

Claim 5 (Currently Amended) The data transfer control circuit according to claim 3, wherein:

 said bus controller sends a state signal indicating the availability of said ~~data bus in~~ unit data buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 6 (Original) The data transfer control circuit according to claim 1, wherein:
 said request signal includes information specifying each unit data bus in said data bus.

Claim 7 (Original) The data transfer control circuit according to claim 1, wherein:
said request signal includes information specifying the number of the unit data buses
in said data bus.

Claim 8 (Currently Amended) An information processing system for carrying out data
transfer by using a plurality of bus masters, comprising:

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a peripheral apparatus;
a data bus connected to a peripheral apparatus, ~~, said data bus having and composed~~
~~of a plurality of unit data buses, into which the data bus is divided and through each of which~~
~~transfers data is transferred concurrently;~~
a plurality of bus masters configured to send a request signal requesting a use of each of
~~said unit data buses bus in units of the unit data bus, and to use using said unit data bus buses~~
~~in unit data buses requested when a request by means of said request signal is granted; and~~
a bus controller configured to split-control ~~said unit data bus buses in unit data buses~~
for said plurality of bus masters by giving a grant signal which grants the use of each of ~~said~~
~~unit data buses bus in units of the unit data bus requested in unit data buses to said bus~~
~~masters in accordance with an said request signal, availability of said data bus in units of the~~
~~unit data bus, wherein~~
the request signal ~~and the grant signal has a data field comprising a plurality of bits,~~
~~each of said plurality of bits corresponding to a respective one of said unit data buses.~~
~~indicate identification or number of the unit data bus divided from the data bus.~~

Claim 9 (Currently Amended) The information processing system according to claim
8, wherein:

said bus controller sends gives the grant signal the use of said data bus to said bus masters upon receipt based on of one of a request and a bus release requesting signal requesting a release of the use of said unit data buses. bus in unit data buses inputted from said bus masters.

Claim 10 (Currently Amended) The information processing system according to claim 8, wherein:

 said bus controller includes a monitor circuit for monitoring the availability of said data bus in unit data buses.

Claim 11 (Currently Amended) The information processing system according to claim 10, wherein:

 said bus controller judges whether said data bus is available in unit data buses of said data bus are available based on a monitoring result by of said monitor circuit, and when said unit data bus is buses are available, said bus controller gives the grant signal of the use of said unit data buses bus to said bus master.

Claim 12 (Currently Amended) The information processing system according to claim 10, wherein:

 said bus controller sends a state signal indicating the availability of said data bus in unit data buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 13 (Original) The information processing system according to claim 8,

wherein:

 said request signal includes information specifying each unit data bus in said data bus.

Claim 14 (Original) The information processing system according to claim 8,

wherein:

 said request signal includes information specifying the number of the unit data buses in said data bus.

Claim 15 (Currently Amended) A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

 generating a request signal requesting a use of each of said unit a data buses bus in units of the unit data bus in each of a plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and composed of a plurality of unit data buses, into which the data bus is divided and through each of which each of said unit data buses transferring data is transferred concurrently;

 sending, in response to said request signal, a grant signal granting the use of each of said unit data buses bus in units of the unit data bus requested in unit data buses to said bus master in accordance with an said request signal; availability of said data bus in units of the unit data bus; and

 occupying said unit data buses bus granted by said grant signal in units of the unit data bus, and carrying out data transfer by using the unit data buses thus occupied, wherein the request signal and the grant signal has a data field comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses. indicate identification or number of the unit data bus divided from the data bus.

Claim 16 (Currently Amended) The method according to claim 15, wherein:

sending of said grant signal includes sending said grant signal based on a bus release
requesting signal requesting a release of said unit data buses. ~~in said grant signal sending~~
~~step, the grant signal of the use of said data bus is given to said bus master upon receipt of~~
~~one of a request and release of the use of said data bus in unit data buses inputted from said~~
~~bus master.~~


Claim 17 (Currently Amended) The method according to claim 15, further comprising:

~~the step of~~
monitoring the availability of said ~~data bus~~ in unit data buses.

Claim 18 (Currently Amended) The method according to claim 17, wherein:

sending of said grant signal includes sending the grant signal based on the availability
of said unit data buses. ~~in said grant signal sending step, whether said data bus is available in~~
~~unit data buses is judged based on a monitoring result in said monitoring step, and when said~~
~~data bus is available, the grant signal of the use of said data bus is given to said bus master.~~

Claim 19 (Currently Amended) The method according to claim 17, wherein further comprising:

sending in said grant signal sending step, a state signal indicating the availability of
said ~~data bus~~ in unit data buses is sent to each of said bus masters, ~~based on a monitoring~~
~~result in said monitoring step.~~

Claim 20 (Currently Amended) The method according to claim 15, wherein:
~~said generating of said request signal includes generating said request signal including one piece of information specifying each unit data bus in said data bus or information specifying the number of the unit data buses in said data bus.~~

Claim 21 (Currently Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, ~~said data bus having and composed of a plurality of unit data buses, into which the data bus is divided and through each of which transfers data is transferred~~ concurrently;

a plurality of bus masters configured to send a request signal requesting a use of ~~each of said unit data buses bus in units of the unit data bus, and to use using said unit data bus buses in unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; when a request by means of said request signal is granted;~~ and

a bus controller configured to split-control ~~said unit data bus buses in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an said request signal, and sending said bus master select signal to each of said bus masters, availability of said data bus in units of the unit data bus, wherein the request signal and the grant signal has a data field comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, the request signal and the grant signal are able to specify each of the unit data bus.~~

Claim 22 (Currently Amended) An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to a peripheral apparatus, said data bus having and composed of a plurality of unit data buses, ~~into which the data bus is divided and through each of which transfers data is transferred~~ concurrently;

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a plurality of bus masters configured to send a request signal requesting a use of each of said unit data buese bus in units of the unit data bus, and to use using said unit data bus buses in unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; when a request by means of said request signal is granted; and

a bus controller configured to split-control said unit data bus buses in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of each of said unit data buses bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an said request signal, and sending said bus master select signal to each of said bus masters, availability of said data bus in units of the unit data bus, wherein the request signal and the grant signal has a data field comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses. the request signal and the grant signal are able to specify each of the unit data bus.

Claim 23 (Currently Amended) A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

generating a request signal requesting a use of each of said unit a data buses bus in units of the unit data bus in each of a plurality of bus masters and sending, in response to a

bus master select signal which indicates the current bus master to which said grant signal is given, said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and ~~composed of a plurality of unit data buses, into which the data bus is divided and through each of which each of said unit data buses transferring data is transferred concurrently;~~

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sending, in response to said request signal, a grant signal granting the use of each of said unit data buses ~~bus in units of the unit data bus requested in unit data buses to said bus master~~ in accordance with ~~an~~ said request signal, and sending said bus master select signal to each of said bus masters; ~~availability of said data bus in units of the unit data bus;~~ and

occupying said unit data buses ~~bus~~ granted by said grant signal ~~in units of the unit data bus,~~ and carrying out data transfer by using the unit data buses thus occupied, wherein the request signal and the grant signal has a data field comprising a plurality of bits, each of said plurality of bits corresponding to one of said unit data buses. ~~the request signal and the grant signal are able to specify each of the unit data bus.~~

Claims 24 - 26. (Cancelled)